MOVELLUS™

Aeonic Integrated Droop Response System

Integrated, Turnkey Droop Response System

Remote Sea of Processors Use Case

Core counts have been increasing steadily since IBM's debut of the Power 4 in 2001, today eclipsing 100 CPU cores and over 1,000 for AI accelerators. While sea of processor architectures feature a stamp and repeat design, per-core workloads aren't always symmetrically balanced. For example, a cloud provider (AI or compute) will rent out individual core clusters to customers for specialized and varied workloads. However, this asymmetry, combined with rapid provisioning changes, can lead to global voltage droops on the SoC resulting in potential logic glitches across the die.

A global voltage droop occurs when there is a sudden rush of switching activity driven by fluctuating workloads, which creates a drop in the supply VDD and might raise the ground voltage level (also known as a ground bounce). A localized voltage droop might result in a global voltage droop and cause setup and hold time violations causing transient glitches and potentially catastrophic mission-mode failures.

System architects can now mitigate droops with integrated droop response systems, which adapt dynamically to voltage droops (IR drops). The technique requires a programmable clock and tightly coupled droop detectors to create a fully self-contained droop response system. Figure 1 shows an example implementation of the Movellus Aeonic Integrated Droop Response system, which can respond to a droop after VDD crosses the pre-set threshold. Design teams can integrate this system IP to reclaim V_{min} margin, which can reduce system power by up to 10% or more, while maintaining or increasing system performance through a tightly-coupled integrated droop response system[1].

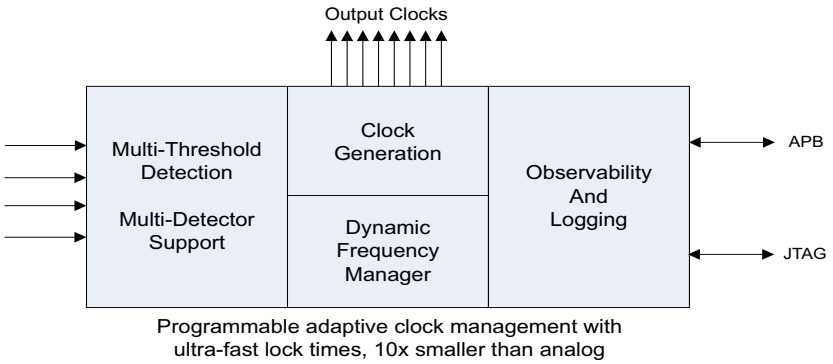

Figure 1. Example Implementation of the Aeonic Integrated Droop Response System

The Movellus Aeonic portfolio offers an integrated droop response system that delivers rapid droop response comprised of two building blocks: one providing adaptive clocking and the other providing droop detection. Together these building blocks mitigate localized timing glitches and improve system power efficiency.

The Movellus Aeonic product portfolio is intrinsically flexible because it is built with synthesizable Verilog. Movellus' expertise lies in converting traditionally analog functions to digital, and this has allowed the company to develop feature-rich digital IP that is synthesizable. Synthesizable IP provides designers with configurable, process-portable IP with a high degree of testability at ATE for a wide range of advanced SoC applications.

The Aeonic digital IP portfolio also enables extensive observability and configurability. The integrated droop response system is outfitted with an APB interface to seamlessly integrate with silicon health and monitoring platforms. It provides rich outbound data, such as droop response sequences and counts, as well as DVFS response and sequences and event codes. Through a programmable interface, architects can configure the number of dynamic and static frequencies based on their droop, DVFS, and core logic clocking needs.

Figure 2 shows an example architecture of a sea of processor SoC with an Aeonic Integrated Droop Response System for global droop support. An architect would place a single adaptive clock IP module on die with multiple detectors to rapidly and globally respond to workload-driven droops. This allows designers to deliver system-wide droop response if a single droop detector trips. The designer also has the ability to set differing thresholds for each detector, which allows a further degree of control on the response when an event is detected.

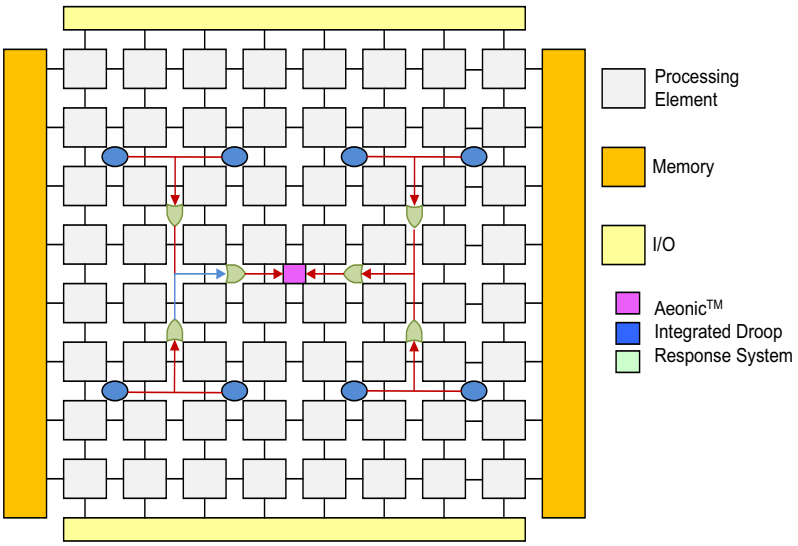

Figure 2. Example SoP SoC with Multiple Detection Elements for Global IR Drop Response

As compute, inference, or training hardware demand continues to grow, silicon designers can improve system power and performance by quickly responding to localized droops. The Movellus Aeonic family provides an integrated turn-key droop response system with near instantaneous frequency shifts and extensive observability - Droops happen, respond in time with the Aeonic Integrated Droop Response System.

References

[1] S. K. Lee, P. N. Whatmough, N. Mulholland, P. Hansen, D. Brooks, and G.-Y. Wei, "A wide dynamic range sparse FC-DNN processor with multi-cycle banked SRAM read and adaptive clocking in 16 nm FinFET," in Proc. IEEE 44th Eur. Solid State Circuits Conf. (ESSCIRC), Sep. 2018, pp. 158-161.