MOVELLUS™

Aeonic Integrated Droop Response System

Integrated, Turnkey Droop Response System

Heterogeneous IP Use Case

Whether you serve the ADAS, PC, or networking market, chances are that your SoC is heterogeneous; containing general processors and application-specific accelerators. Your solution might have a systolic array for convolutions, a cluster of CPUs for application code, or a look-aside crypto engine for packet security. While application-specific accelerators significantly improve performance and power efficiency, they can face localized droops from dynamic workloads or induce droops under heavy load.

A localized voltage droop occurs when there is a sudden rush of switching activity driven by fluctuating workloads, which creates a drop in the supply VDD and might raise the ground voltage level (also known as a ground bounce). A localized voltage droop might result in setup and hold time violations causing transient glitches and potentially catastrophic mission-mode failures.

System architects can now mitigate droops with integrated droop response systems, which adapt dynamically to voltage droops (IR drops). The technique requires a programmable clock and a tightly coupled droop detector to create a fully self-contained droop response system. Figure 1 shows an example implementation of the Movellus Aeonic Integrated Droop Response system, which can respond to a droop after VDD crosses the pre-set threshold. Design teams can integrate this system IP to reclaim V_{min} margin, which can reduce system power by up to 10% or more, while maintaining or increasing system performance through a tightly-coupled integrated droop response system[1].

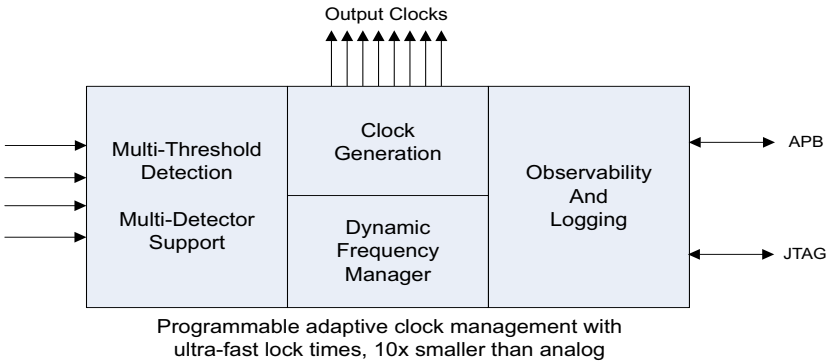

Figure 1. Example Implementation of the Aeonic Integrated Droop Response System

The Movellus Aeonic portfolio offers an integrated droop response system that delivers rapid droop response comprised of two building blocks: one providing adaptive clocking and the other providing droop detection. Together these building blocks mitigate localized timing glitches and improve system power efficiency.

The Movellus Aeonic product portfolio is intrinsically flexible because it is built with synthesizable Verilog. Movellus' expertise lies in converting traditionally analog functions to digital, and this has allowed the company to develop feature-rich digital IP that is synthesizable. Synthesizable IP provides designers with configurable, process-portable IP with a high degree of testability at ATE for a wide range of advanced SoC applications.

The Aeonic digital IP portfolio also enables extensive observability and configurability. The integrated droop response system is outfitted with an APB interface to seamlessly integrate with silicon health and monitoring platforms. It provides rich outbound data, such as droop response sequences and counts, as well as DVFS response and sequences and event codes. Through a programmable interface, architects can configure the number of dynamic and static frequencies based on their droop, DVFS, and core logic clocking needs.

Figure 2 shows an example architecture of an ADAS processor with the Aeonic Integrated Droop Response System for localized droop support. An architect would place an integrated system within an application-specific sub-block or accelerator to respond to workload-driven localized droops. This allows designers to deliver localized and independent droop response without altering the performance of neighboring IP blocks.

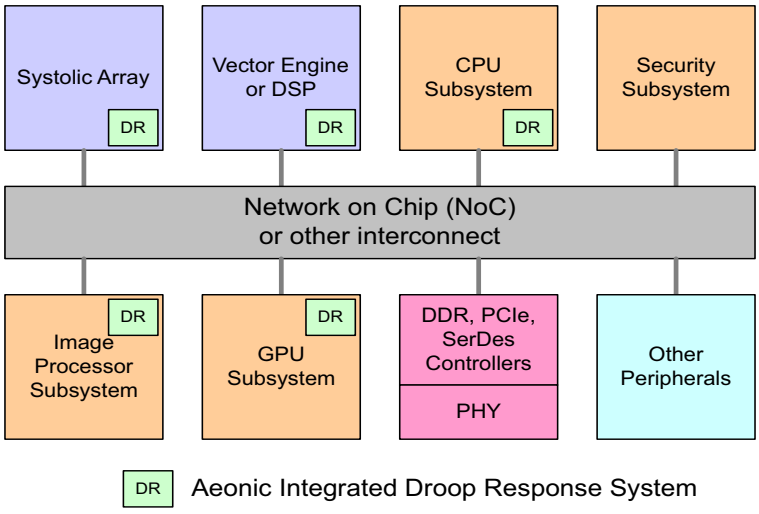

Figure 2. Example SoP SoC with Multiple Detection Elements for Global IR Drop Response

For distributed clock solutions, customers can integrate multiple droop response systems per chip to manage the settings and behavior per subsystem. Large silicon solutions often face significant process variation across a large die (OCV), leading to uneven droop behavior across processing elements. A distributed solution allows architects to take a fine-grain response approach per subsystem, instead of a single droop profile for the entire chip. Additionally, the distributed systems will provide valuable insight on droop, DVFS, and clocking behavior of that IP subsystem during test and in the field.

Being much smaller than traditional analog solutions, allows designers to easily instantiate the IP at the granularity required without any significant impact to the area. And as designs move to finer process geometries (e.g., 5 and 3nm), the Aeonic Integrated Droop Response System area continues to scale - one of the many advantages of implementing clock generation digitally vs. a traditional analog approach.

Application-specific accelerators deliver leaps in power and performance, and are necessary for comprehensive solutions in the ADAS, 5G, and data center networking markets. However, these same accelerators face varying workloads and utilization rates that lead to localized droops. Adaptive clocking solutions, such as the Aeonic Integrated Droop Response Platform, swiftly respond to droop, resulting in more reliable performance with dynamic workloads. Droops will happen - respond in time with the Aeonic Integrated Droop Response System.

References

[1] S. K. Lee, P. N. Whatmough, N. Mulholland, P. Hansen, D. Brooks, and G.-Y. Wei, "A wide dynamic range sparse FC-DNN processor with multi-cycle banked SRAM read and adaptive clocking in 16 nm FinFET," in Proc. IEEE 44th Eur. Solid State Circuits Conf. (ESSCIRC), Sep. 2018, pp. 158-161.