Sea of Processors Use Case

Core counts have been increasing steadily since IBM's debut of the Power 4 in 2001, eclipsing 100 CPU cores and over 1,000 for AI accelerators. While sea of processor architectures feature a stamp and repeat design, per-core workloads aren't always going to be symmetrically balanced. For example, a cloud provider (AI or compute) will rent out individual core clusters to customers for specialized and varied workloads. OEMs and data center operators can tackle this asymmetry through fine-grain, per-cluster performance turning.

Many compute cores scale performance by scaling frequency up or down. Design engineers can use a single clock generator and post-divide the outputs or implement many area-efficient clock generators. However, as core counts keep rising, a single clock source and many post dividers increase clock routing congestion and force compute clusters to rise and fall in parallel based on the source clock generator's behavior. Distributed clocking addresses these issues by providing fine grained, independent frequency control on a per core, per cluster or per tile basis. However, in order to do this the overall efficiency of the clock generation solution matters.

Digital clock generation enables distributed clocking. Digital clock generators are smaller than their analog counterparts, run on core voltage and continue to scale with process. The Aeonic Generate CGM is a synthesizable clock generation solution that features eight output ports for sea of processor SoCs. It is programmable due to its digital building blocks and features enhanced observability for live mission mode telemetry.

Figure 1 shows an example of a sea of processor SoC with distributed clocking. Customers can integrate many CGMs per chip that supplies independently controlled frequencies to multiple compute cores. Each CGM is fully programmable, and this flexibility translates to fine-grain performance tuning per processing cluster.

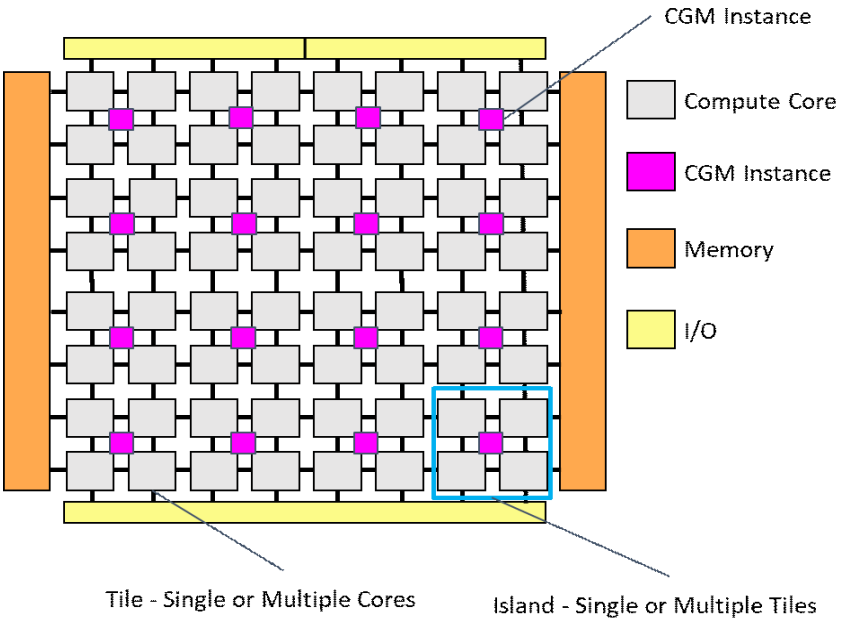

Figure 1. Sea of Processors Example Architecture with Distributed Clocking

The Movellus Aeonic Generate product family is intrinsically flexible because it is built with synthesizable Verilog. Movellus' expertise lies in converting traditionally analog functions to digital and this has allowed the company to develop feature-rich digital IP that is synthesizable. This provides designers with configurable, scannable, and process-portable IP for Sea of Processor (SoP) applications.

For distributed clock solutions, the Aeonic Generate CGM simplifies implementation. It reduces clock routing difficulty for physical design because it is closer to the core logic and reduces floor planning headaches since it is synthesizable. The Generate CGM is up to 8x smaller, preventing clocking area bloat for distributed solutions. As designs move to finer process geometries (e.g., 5 and 3nm), this area difference only widens due to improved scaling of digital logic vs. analog.

As compute, inference, or training as a service continues to grow, silicon designers can maintain user experience while still optimizing power consumption by offering fine-grain performance tuning per compute cluster. Aeonic Generate CGMs provide a clock generation solution that makes distributed clocking a reality with up to an 8x reduction in area overhead, mission-mode programmability, and core-voltage-only supply needs. Consider Aeonic Generate for your programmable, flexible, and distributed clocking needs to maximize user experience and system performance.